

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE (REV. 7-80) PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) DATE MAILED: March 7, 2002	APPT. DOCKET NO. 010544	SERIAL NO. 10/010,199
	APPLICANT Butler, et al.	
	FILING DATE December 4, 2001	GROUP 2133

U.S. PATENT DOCUMENTS

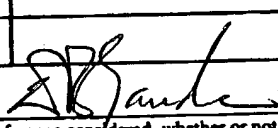
EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPRO- PRIATE
	A1						
	A2						
	A3						
	A4						
	A5						

RECEIVED
MAR 22 2002
Technology Center 2100

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
	B1						
	B2						
	B3						
	B4						
	B5						
	B6						
	B7						

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Page, Etc.)

DG	C1	Rizzo, Luigi., <i>On the feasibility of software FEC</i> ; Dip. di Ingegneria dell'Informazione, Universita di Pisa, via Diotallevi 2 - 56126 Pisa (Italy)
	C2	
EXAMINER		
	DATE CONSIDERED 8/19/2004	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
(REV. 7-80) PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(Use several sheets if necessary)

DATE MAILED: November 19, 2003

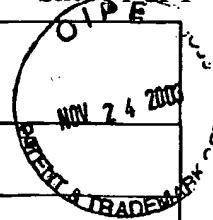
ATTY. DOCKET NO.
010544

SERIAL NO.
10/010,199...

APPLICANT
Butler et al.

FILING DATE
December 4, 2001

GROUP
~~2184~~ 2133



U.S. PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPRO- PRIATE
	A1						
	A2						
	A3						
	A4						
	A5						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
DG	B1	0 4 0 7 1 0 1	A2	01/09/91	EP	Digital Equipment Corp.	G11B 20/18
	B2						
	B3						

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Page, Etc.)

DG	C1	Katayama, Y et al: "One-Shot Reed-Solomon Decoding For High-Performance Dependable Systems", 2000 IEEE International Networks, NY, USA, June 25, 2000, pages 390-399.
DG	C2	Alzahrani, F et al: "On-Chip TEC-QED ECC For Ultra-Large, Single-Chip Memory Systems", Proceedings IEEE International Conference On Computer Design, October 10, 1994, pages 132-137.
DG	C3	Franklin, M et al: "Theory and Techniques For Testing Check Bits Of Rams With On-Chip ECC", IEICE Transactions On Information and Systems, Tokyo, Japan, Volume E76-D, No. 10, October 1, 1993, pages 1243-1252.
DG	C4	Nagvajara, P : "Multichip Module Diagnosis, Electro/94 International Conference Proceedings, Boston, MA, IEEE, USA. Combined Volumes, May 10, 1994, pages 793-802.
EXAMINER		DATE CONSIDERED
[Signature]		8/19/2004
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		

BEST AVAILABLE COPY